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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/729,732	12/05/2003	Tazrien Kamal	H1983	1323

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EXAMINER	
PERT, EVAN T	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 05/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/729,732	KAMAL ET AL.	
	Examiner	Art Unit	
	Evan Pert	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *21-31* is/are allowed.

6)☒ Claim(s) *1-11 and 14-20* is/are rejected.

7)☒ Claim(s) *12 and 13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 December 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1203 & 0704*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Fig. 4 uses "420" to delineate both "word line(s)" and "location(s)" of "bit(s)," which are significantly different "parts" because a "bit 420" is not "located" or stored in the "word line 420."

While the informality related to "420" in Fig. 4 should readily be understood by anyone of ordinary skill in the art, correction of duplicate numbering is required to comply with 37 CFR 1.84(p)(4).

2. Step "510" of Fig. 5 has the typographical error "SAPCER" (i.e. should read –spacer--). Correction of this informality is required.

Specification

3. The disclosure is objected to because of the following informalities:

- At p. 5, line 12, "sized" should seemingly read --sizes--.
- In the sentence at lines 16-19 of p. 12, "so that the during" should seemingly read --so that during--.

Appropriate corrections are required.

Claim Objections

4. Claim 4 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. That is, "claim 4" refers to "claim 5" which is not a "previous claim."

5. In claim 13, there is a lack of antecedent basis for the claim term "sacrificial oxide layer," although this layer is understood to be the "second insulating layer" that gets "removed" as in claim 12.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-8, 14-16 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. (US 6,524,913 B1) in view of Yang et al. (US 5,418,176).

Regarding claim 1, the Lin et al. reference discloses a method of forming at least a portion of a dual bit memory core array upon a semiconductor substrate [col. 2, lines 5-14], the method comprising: forming a charge trapping dielectric layer over the substrate (i.e. form 238 in Fig. 2A over 200); forming a hardmask (240) over the charge trapping dielectric layer; patteming the hardmask to form a plurality of hardmask features having a first spacing therebetween (patterned 240 is seen in Fig. 2A with a first spacing); forming a spacer material over the patterned hardmask (the layer that formed spacer 241 was anisotropically etched to arrive at Fig. 2B); patterning the spacer material to form spacers adjacent the hardmask features and defining a second spacing between the hardmask features that is less than the first spacing (i.e. the spacing in Fig. 2B is lessened compared to Fig. 2A); performing a bitline implant (244) through the charge trapping dielectric (238 = 230/220/210 in Fig. 2B) to establish

buried bitlines (250) within the substrate (200) having a width corresponding to the second spacing (e.g. col. 3, lines 54-61); removing the patterned spacers (e.g. claim 13); forming a wordline material (254) over the charge trapping dielectric layer (220); and patterning the wordline material to form wordlines that overlie the bitlines (i.e. wordlines 254 are patterned and overlie bit-lines 250).

Regarding claim 6, the forming a charge trapping dielectric layer comprises: forming a first insulating layer over the semiconductor substrate (210); forming a charge trapping layer over the first insulating layer (220); and forming a second insulating layer over the charge trapping layer (230).

Regarding claim 7, the first and second insulating layers comprise silicon dioxide (col. 3, lines 13-14).

Regarding claim 8, the charge-trapping layer comprises silicon nitride col. 3, lines 13-15).

Regarding claim 14, "at least one of" the "hardmask and spacers" are "formed of nitride or poly-based materials" (e.g. the patterned hardmask 240 is polysilicon per col. 3, line 24).

Regarding claim 16, the wordlines are oriented at substantially right angles relative to the buried bitlines (e.g. word lines 254 are perpendicular to bit lines 250 in Fig. 2E).

Regarding claim 20, the substrate inherently "comprises silicon" because the "silicon oxide layer 210" is "preferably performed by thermal oxidation" of the substrate, the "substrate" having "lattice structure" [col. 3, lines 16-35].

Regarding claims 1-8, 14-16 and 20, the Lin et al. reference is silent about "removing the spacers *and the patterned hardmask,*" because the hardmask is not disclosed as "removed," and is only disclosed as at least partly remaining (e.g. Fig. 2E or claim 13), wherein the meaning of "removing the patterned hardmask and spacers" in claim 1 is reasonably taken to mean that after the "removing," the "pattered hardmask and spacers" do not remain, as opposed to being *partly-removed*, or *patterned*, as seen in Fig. 2D of Lin et al. where 240a is not formed by "removing 240," but rather by "patterning 240," which is a partial removal that do not encompass the plain meaning of "removed" as originally filed.

The Yang et al. reference is directed at narrower bit lines than can be achieved by photolithography, using sacrificial spacers [col. 3, lines 8-46, particularly lines 43-46], which is the kind of bit line needed in Lin et al. [e.g. a narrower bit line increases distance between two data bits per col. 4, lines 31-38].

It would have been obvious to one of ordinary skill in the art at the time of claimed invention to adopt the teachings of the Yang et al. reference in practicing the invention disclosed in the Lin et al. reference, motivated to select appropriate implant and masking conditions because "in manufacturing semiconductor devices, an objective is to make all devices as small as possible" per col. 3, lines 12-14 of Yang et al.:

One would be motivated to adopt the teachings of forming narrow bit lines in the Yang et al. reference in forming bitlines of the Lin et al. reference, because bit lines as disclosed in the Yang et al. reference can be formed "narrower than the narrowest possible compared to directly using the maximum resolution of the photolithographic process" [col. 3, lines 42-46].

In Yang et al. the spacers and hardmask are removed (Fig. 8 to 9), which one of ordinary skill in the art would need to do using Yang et al.'s exemplary mask materials of oxide or nitride, in place of the polysilicon mask suggested by Lin et al..

Regarding claims 2-5 and 15, in adopting the suggestions of Yang et al. in Lin et al., such as "removing the hardmask and the spacers," one would also follow the direction of Yang et al. for general matters of which Lin et al. is silent:

Regarding claim 2, the substrate is "preferably p-type" and the implantation is "typically achieved by implanting n-type ions" [col. 3, lines 46-47].

Regarding claim 3, the n-type dopant for the bit-line is "preferably arsenic" [col. 3, line 47].

Regarding claim 4, the dosage is in the range of "5E13 to 5E16 atoms/cm2" [col. 3, line 49].

Regarding claim 5, the energy level is "20 to 150 KeV" [col. 3, line 48].

Regarding claim 15, the Yang et al. and Lin et al. references are silent about specific numerical values of the actual sizes of bit lines that are "smaller than achievable by photolithography," yet one of ordinary skill in the art would be motivated to make them as small as possible [col. 3, lines 12-14], yet not so small that the current-carrying capability is unacceptably degraded [MPEP 2144], since it is rudimentary knowledge that sizes of conductors have lower functional bounds.

The range of "40 to 100 nano-meters" as claimed is not patentable because there is nothing unexpected about the size range and the size would be arrived at by routine experimentation when miniaturizing the device disclosed in Lin et al., as directed by the Yang et al. reference. Furthermore, the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is to be based upon a particular chosen dimension or other variable recited in a claim, the Applicant must show that the chosen values of the dimension or other variable are critical. In re Woodruff, 919 F .2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

8. Claims 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Yang et al., as applied to claim 6 above, and further in view of Cheng-Sheng et al. (1990 IEEE article entitled "A Scaling Methodology for Oxide-Nitride-Oxide Interpoly Dielectric for EPROM Applications").

The Lin et al. and Yang et al. references are silent about explicit "thicknesses" for an exemplary ONO charge trapping structure:

The Cheng-Sheng article explains that the advantage of "the three-layer nature of ONO" is that "ONO offers the possibility of maximizing the charge retention capability by varying the individual thicknesses" [upper right p. 1439].

The Cheng-Sheng article also indicates that prior art ONO "reported in the literature" is comparable to "50-100 angstroms bottom oxide, 100-200 angstroms nitride, and 50-100 angstroms top oxide" [II. Experiments].

It would have been obvious to one of ordinary skill in the art at the time of the claimed invention to pick thicknesses of the prior art suggested by Cheng-Sheng et al., or to experiment with thicknesses to "maximize charge retention" as explained by the Cheng-Sheng et al. reference.

Furthermore, the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is to be based upon a particular chosen dimension, applicant must show that the chosen values of the dimension are critical. In re Woodruff, 919 F .2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

9. Claims 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Yang et al., as applied to claim 1 above, and further in view of Kamal et al. (US 6,884,681).

The Lin et al. and Yang et al. references are silent about performing a prior art "threshold adjustment implant" before forming the charge-trapping layer 238.

The Kamal et al. reference discloses the advantage of a threshold adjustment implant before depositing the charge-trapping dielectric [col. 4, lines 52-58], wherein the a p-type material such as boron is implanted at a greater concentration than the p-type substrate.

It would have been obvious to one of ordinary skill in the art at the time of the claimed invention to adopt the threshold adjustment implant disclosed by the Kamal et al. reference, motivated to "assist in the control of the threshold voltage of the memory cell" [col. 4, lines 56-57 of Kamal et al.].

Allowable Subject Matter

10. Claims 12 and 13 are objected to as being dependent upon a rejected base claim, as well as the informality in claim 13 noted in item 5 above, but would otherwise be allowable.

11. Claims 21-31 are allowed.

12. The following is a statement of reasons for the indication of allowable subject matter:

Applicant's invention can be distinguished from prior art by the acts of "forming a layer of sacrificial material..." and then "forming a remaining portion..." (i.e. claims 21-31), or, stated alternatively, by acts of "removing a second insulating layer of a charge trapping layer" and then "re-applying the second insulating layer..." (i.e. claims 12-13).

While prior art recognizes damage to the top oxide of ONO in semiconductor device manufacturing, the damage is avoided by "extra process steps to protect the ONO," or "alternatively," by using "cleaning solutions that do not damage oxide" (e.g. see [0007] of US 2003/0232507 A1).

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US 6,872,609 is cited as the result of 10/755,430, indicated as "related" by applicant [e.g. preliminary amendment filed 7-30-04].

Mori et al. (1991 IEEE article) is cited for discussing the prior art experimentation of thicknesses of the bottom oxide, middle nitride, and top oxide of an ONO charge trapping layer, particularly relevant to claims 6-11 and claims 22-29.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Evan Pert whose telephone number is 571-272-1969. The examiner can normally be reached on M-F (7:30AM-3:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ETP
May 9, 2005

EVAN PERT
PRIMARY EXAMINER